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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,365	10/09/2002	Robert W. Bassett	BUR920010209	7874

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/065,365	BASSETT ET AL.
	Examiner	Art Unit
	Cynthia Britt	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 is/are rejected.

7)☒ Claim(s) 1 and 10 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 October 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-10 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on October 28, 2002 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Specification

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms, which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are:

Page 3 line 2 "such electronic tester"

Page 3 line 7 "ain short"

Page 4 line 3 "much less channels"

Page 4 line 6 "pins containing with input receivers"

The examiner suggests careful proofreading to ensure obvious spelling, grammatical, and typographical errors are corrected. Appropriate correction is required.

The disclosure is objected to because of the following informalities: The use of the term measures is unclear. This term could be interpreted in a number of ways: "An

action or steps taken as a means to an end; an expedient. Often used in the plural" "To estimate by evaluation or comparison" "To consider or choose with care; weigh" "To take, have, or allow a measurement of". The examiner, for purposes of examination will assume measures to be intended as steps taken. If this interpretation is not the intended use, perhaps replacing the term 'measures' with 'measurement' would help to clarify the present invention. This term is unclear in the following places in the specification:

Page 3 lines 4 and 5: Measures within the driver tests were ignored when the measured pin was not active in a particular group.

Page 10 lines 22 and 23: The banking method used in the present invention handles the measures within the external I/O driver tests in the same fashion as the earlier method.

Page 12 lines 20 and 21:This method allows all pins that are continuously contacted plus all pins in a given bank to have stimuli and measures within the same test pattern.

Page 13 lines 20 and 21: Each test in the test patterns may contain any number of stimuli and measures on the external I/O pins.

This usage also occurs numerous times on page 15.

Appropriate correction is required.

Claim Objections

Claim 1 is objected to because of the following informalities: In line 10, "channels then pins", 'then should be 'than'. Appropriate correction is required.

Claim 10 is objected to because of the following informalities: In lines 6 and 7, "channels then pins", 'then should be 'than'. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 8, the use of the term measures as discussed above, is unclear. This term could be interpreted in a number of ways: "An action or steps taken as a means to an end; an expedient. Often used in the plural" "To estimate by evaluation or comparison" "To consider or choose with care; weigh" "To take, have, or allow a measurement of". The examiner, for purposes of examination will assume measures to be intended as steps taken. If this interpretation is not the intended use, perhaps replacing the term 'measures' with 'measurement' would help to clarify the present invention. This term is unclear in the following places in the specification:

Page 3 lines 4 and 5: Measures within the driver tests were ignored when the measured pin was not active in a particular group.

Page 10 lines 22 and 23: The banking method used in the present invention handles the measures within the external I/O driver tests in the same fashion as the earlier method.

Page 12 lines 20 and 21:This method allows all pins that are continuously contacted plus all pins in a given bank to have stimuli and measures within the same test pattern.

Page 13 lines 20 and 21: Each test in the test patterns may contain any number of stimuli and measures on the external I/O pins.

This usage also occurs numeroûs times on page 15.

Claims 2-9 are dependent on claim 1 and therefore inherit the 35 U.S.C. 112, second paragraph rejection and issues of the independent claim 1. As such each dependent claim may not be further treated on individual merit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 are rejected under 35 U.S.C. 103(a) as being obvious over Ellison et al. U.S. Patent No. 6,448,796 in view of Schnurmann U.S. Patten No. 5,348,759.

As per claims 1, and 2, Ellison et al. substantially teach the claimed method of parametric testing of high pin count circuits with low channel testers by the following; 1) identify all the types of common module drivers which can be grouped together at the tester interface board (TIB) or driver interface board (DIB). Grouping common drivers allows the parametric tests of the pins to use the same test criteria, and thus have a consistent test for each of the shared pins at the connections. The test equipment can treat a shared pin as a consistent known entity and does not need to differentiate results based on patterns and type of driver. Typical designs tend to use common drivers across large busses and system interfaces, so this grouping is generally likely to be easily performed. 2) Insert logic driver controls in the design to allow only a single grouped driver of a grouping or bank to be active at any given test vector (column 3 line 50 through column 4 line 33, figure 3, claim 1). Not explicitly disclosed is applying test patterns from the tester.

However, in an analogous art, Schnurmann teaches a method for testing integrated circuits with less channels on the tester than pins on the integrated circuit and sending a test pattern through the pins. During operation, a plurality of terminal pins are connected to one channel. Each test pattern forces either a 0 or 1 to every input pin (column 8 lines 16-25, abstract, claims 1-5). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the tester of Schnurmann with the method of Ellison et al. This would have been obvious as suggested by Ellison et al. (column 2 lines 7-15) in order to ensure high test coverage on high pin count products.

As per claim 3, Ellison et al. teach that grouping I/Os assists in being able to "fit " the device on a given test platform, but selective grouping, taking into account the physical I/O assignments and location, aids in minimizing test escapes to the field. Column 3 lines 5-13

As per claims 4-8, Ellison et al. teach Inserting driver logic controls is done at the chip design level, and requires I/O bank logic to uniquely control selected banks of I/O drivers. Taking the groups of common drivers into account, a suitable number of drivers are provided to facilitate an enable control function so as to allow specific control of any given driver bank. This design is then used to uniquely control the driver banks, when test vectors are created, by allowing selectively enabling drivers banks, and to control the number of I/Os which are switched for testing. (Column 3 line 66 through column 4 line 9, FIG. 3)

Claims 10 are rejected under 35 U.S.C. 103(a) as being obvious over Ellison et al. U.S. Patent No. 6,448,796 in view of Godiwala et al. U.S. Patent No. 5,712,858

As per claim 10, Ellison et al. substantially teach the claimed method of parametric testing of high pin count circuits with low channel testers by the following; 1) identify all the types of common module drivers which can be grouped together at the tester interface board (TIB) or driver interface board (DIB). Grouping common drivers allows the parametric tests of the pins to use the same test criteria, and thus have a consistent test for each of the shared pins at the connections. The test equipment can treat a shared pin as a consistent known entity and does not need to differentiate results based on patterns and type of driver. Typical designs tend to use common drivers across large busses and system interfaces, so this grouping is generally likely to be easily performed. 2) Insert logic driver controls in the design to allow only a single grouped driver of a grouping or bank to be active at any given test vector (column 3 line 50 through column 4 line 33, figure 3, claim 1). Not explicitly disclosed is applying test patterns to the ASIC from the tester.

However, in an analogous art, Godiwala et al. teach an electronic testing system for ASIC integrated circuits can test an electronic device which has more signal pins or pads (i.e., contacts) than the maximum number of tester probes. The testing system connects the contacts to the tester such that groups of contacts share individual tester signal lines. The testing system uses special selector logic on the device to be tested to determine which particular contacts of the groups are "currently output active", or capable of transmitting data. At each step in the testing procedure, the system can

vary the sets of contacts hich are chosen to be currently output active, thereby resulting in a high percentage of the possible states of the device being tested. The test system can apply precision voltage and current signals to the DUT contacts, and can measure precision voltage and current responses on those contacts to those applied signals. More specifically, the DUT is `exercised` by the test system by the application of a pattern of `ones` and `zeros`, or high and low voltages, known as a stimulus vector, on a selected set of the tester probes associated with that vector. Then the test system measures the DUTs output pattern of high and lows on a selected set of the DUT contacts associated with that vector, and compares this pattern to a predetermined, i.e. expected, pattern for that vector. (Column 4 lines 16-32, Abstract, claims 1-5,Figures 5,and 6) Therefore it would have been obvious to a person having ordinary skill in the art to have used the method of Ellison et al. with the tester of Godiwala et al. This would have been obvious as suggested by Ellison et al. (column 2 lines 7-15) in order to ensure high test coverage on high pin count products.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,658,613 Rearick et al.

This patent teaches testing procedures, including: (1) connecting an ATE to less than all of the pins of an IC device; (2) connecting multiple pins of an IC device to a single ATE test channel; (3) testing the IC device in multiple passes of the ATE, with

each pass testing a subset of the pins of the entire IC device; (4) testing the device at less than maximum frequency, and; (5) limiting, through design implementation, the pin count and/or frequency of the IC device to accommodate existing ATE, among others.

U.S. Patent No. 6,556,938 Rohrbaugh et al.

This patent teaches testing procedures, including: (1) connecting an ATE to less than all of the pins of an IC device; (2) connecting multiple pins of an IC device to a single ATE test channel; (3) testing the IC device in multiple passes of the ATE, with each pass testing a subset of the pins of the entire IC device; (4) testing the device at less than maximum frequency, and; (5) limiting, through design implementation, the pin count and/or frequency of the IC device to accommodate existing ATE, among others.

EP 0388790 A2 Littlebury

This patent teaches an interface apparatus for coupling a multi-channel tester to a high pin count logic circuit for use in testing the logic circuit is provided wherein a plurality of terminal electronics units are coupled to each test channel of the multi-channel tester. Some of the terminal electronics units are coupled to each other in parallel by at least one stimulus shift register, which serves to divide a serial stimulus vector among the terminal electronics units, and one response shift register, which serve to assemble the response data from several terminal electronics units into a serial response vector. The serial stimulus vector is generated, and the multi-channel tester analyzes the serial response vector. The apparatus is capable of operating in one of a

plurality of modes used for functional testing, parametric testing, and high speed scan path testing of the logic circuit.

"*A Study of the Optimization of DC Parametric Tests*" Chang, J.M. International Test Conference 1990 Proceedings: 10-14 Sept. 1990 pages 478 - 487 Inspec Accession Number: 3976214

This paper teaches that in application-specific integrated circuit (ASIC) testing, the time consumed by DC parametric tests is much greater than that needed for functional tests, taking a significant part of the total testing time. A study on how to optimize DC parametric testing is presented. An optimal algorithm for selecting preconditioning addresses which results in an efficient use of automatic test equipment (ATE) is introduced. The idea is to minimize the total time spent using the parametric measurement unit, i.e., to do parallel measurement as much as possible. Benchmark results comparing this approach with a traditional method are presented. In addition, several key factors which affect the actual testing efficiency are discussed. Through the power of ATPG (automatic test pattern generation), not only is the speed of generating test programs increased, but the quality of the programs generated is improved.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CB

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Art Unit 2133

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